REMARKS

This Amendment is responsive to the Final Office Action dated October 20, 2005. All objections and rejections of the Examiner are respectfully traversed. Reconsideration and further examination is respectfully requested.

In paragraphs 2-25 of the Office Action the Examiner again rejected claims 1-33 under 35 U.S.C. 102(b), citing United States patent number 4,817,080 of Soha ("Soha"). Applicants respectfully traverse these rejections.

Nowhere in Soha is there disclosed or suggested any system or method for monitoring a network including:

> reading an entry of a memory device, the entry of the memory device containing ***both a first statistical value and a second statistical value, wherein the entry is a single memory location of the memory device***, wherein the first statistical value includes a ***packet count***, and wherein the second statistical value includes a ***byte count***;
>
> determining a third statistical value based on at least one of a content of the at least one data packet, the first statistical value, and the second statistical value, ***wherein the third statistical value includes a new value of the packet count and a new value of the byte count***;
>
> ***storing the entire set of bits of the determined third statistical value into the entry of the memory device***; and
>
> ***wherein said reading, determining and storing are performed without interruption***. (emphasis added)

as in the present independent claim 1. Independent claims 12 and 23 include analogous features. In contrast, Soha describes a system in which packet and byte counters are stored in separate memory locations, and in which the packet and byte counters are updated in separate, independent operations. As stated in Soha at column 6 in lines 55 - 69, the microprocessor operates in response to a received packet by "by fetching the contents of ***a predetermined location in the packet memory 50 that serves as a packet counter***, incrementing those contents,

and writing them back into that location" (emphasis added). This section describes clearly that, as shown in step 58 of Fig. 5, the Soha system uses a first memory entry ("a predetermined location") located within the counter section of packet memory 50 to store a packet counter. The operation of the Soha system at step 58 is solely related to updating the packet counter stored at that memory location within the counter section of the packet memory 50. In this way Soha expressly teaches a first independent step of writing a new value to a packet counter that is performed prior to further processing of the received packet, including the determination of a new byte count value to be used to write to a separate byte counter.

In a separate, independent step 62 shown in Fig. 5 in Soha, a second, subsequent operation, is performed after the writing of the packet count in step 58. In this separate step, the Soha microprocessor fetches a count of the number of bytes in the received packet, and writes a new value to another location within the packet memory 50 that is used as a counter for a byte counter. This is confirmed in column 7 lines 10-14 of Soha, which states that the "microprocessor fetches the contents of ***that location***, adds to them the packet byte count that it fetched from the packet-storage part of the packet memory 50, and ***returns the results to that location***" (emphasis added). The above cited sections of Soha expressly teach the maintenance of two separate memory locations within the packet memory 50, that are used to separately store packet and byte counters, and that are updated in separate, independent steps.

That the packet and byte counters of Soha are independently stored in two separate memory locations through two independent steps is further taught at line 15 of column 7, which states:

> In both of the ***operations*** represented by levels 58 and 62, the location of the counter to be updated was predetermined; the program memory 53 contains the ***locations*** of the ***packet and byte counters***, so the microprocessor does not have to employ the look-up

engine 54 and the look-up table 56 in order to locate the counter of interest. (emphasis added)

Thus it is clear that the packet and byte counters of Soha consist of separate memory locations that are updated and stored in separate, independent operations upon receipt of a packet.

For the above reasons, Applicants respectfully urge that Soha does not disclose or suggest all the features of the present independent claims 1, 12 and 23. Accordingly, Soha does not anticipate the present independent claims 1, 12 and 23 under 35 U.S.C. 102. As the remaining claims depend either directly or indirectly from claims 1, 12, and 23, they are respectfully believed to be patentable over Soha for at least the same reasons.

In paragraphs 26-32 of the Office Action, the Examiner rejected claims 34-39 as being obvious under 35 U.S.C. 103, citing Soha in combination with United States patent number 6,687,247 of Wilford et al. ("Wilford et al.") Applicants respectfully traverse these rejections.

Nowhere in the combination of Soha and Wilford et al. is there disclosed or suggested any system or method for monitoring a network, that includes:

> reading an entry of a memory device, the entry of the memory device containing ***both a first statistical value and a second statistical value, wherein the entry is a single memory location of the memory device***, wherein the first statistical value includes a ***packet count***, and wherein the second statistical value includes a ***byte count***;
>
> determining a third statistical value based on at least one of a content of the at least one data packet, the first statistical value, and the second statistical value, ***wherein the third statistical value includes a new value of the packet count and a new value of the byte count***;
>
> ***storing the entire set of bits of the determined third statistical value into the entry of the memory device***; and
>
> ***wherein said reading, determining and storing are performed without interruption***. (emphasis added)

as in the present independent claims 1, 12 and 23, from which claims 34-39 depend. As discussed above with regard to the rejections under 35 U.S.C. 102, Soha teaches a system in which tag fields may be combined with pointers, but in which byte and packet counters are expressly described as stored by separate steps in different, independently maintained memory locations. As noted in Applicants' previous response, beginning at line 43 of column 52 Wilford et al., describe a Committed Access Rate (CAR) Statistics Module beginning that receives data from the Token Bucket Module in Fig. 30. With regard to counters, Wilford et al. state as follows:

> The CAR Statistics Module keeps a count of all packets and bytes passed and dropped per token bucket. The packet ***counters*** are 32 bits and byte ***counters*** 40 bits. The drop ***counters*** will be approximately 4 bits smaller as we should not be dropping at full line rate for very long so packet drop ***counters*** are 28 bits and byte drop counters are 36 bits. All of these ***counters*** should saturate (i.e. not roll over) and clear when read by the CPU.

Wilford et al. provide no other discussion of counters. Accordingly, the teaching of Wilford et al. regarding packet count and byte count statistics is limited to providing counters of some kind, without a hint or suggestion as to the specific structure or operation of the counters, beyond suggested sizes, and that the counters should not roll over. Thus Wilford et al. provides no significant teaching regarding the above set forth features of the present independent claims beyond that discussed above in Soha.

For the above reasons, Applicants respectfully urge that the combination of Soha and Wilford et al. fails to disclose or suggest all the features of the present independent claims 1, 12 and 23, from which claims 34-39 depend. Accordingly, the combination of Soha and Wilford et al. does not support a *prima facie* case of obviousness with regard to the present independent

claims 1, 12 and 23 under 35 U.S.C. 103. As to claims 34-39, they each depend either directly or indirectly from independent claims 1, 12 and 23, and are respectfully believed to be patentable over the combination of Soha and Wilford et al. for at least the same reasons. Reconsideration of all pending claims is respectfully requested.

In view of the above, Applicants respectfully urge that the present claims are allowable, and respectfully request that all rejections of the Office Action be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 617-630-1131 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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